color reduction means in electrical [communicatiion] communication with said universal video input selector means for [reducing] producing digital signals from said image components [from] and reducing said digital [primary color] signals to a monochrome display image when [driving a] said video signal is a color signal and said flat panel display is a monochrome display [into a display image], and otherwise passing said digital signals through without reduction;

[stroage] storage means in electrical communication with said universal video input selector means and said color reduction means for storing said monochrome display image when said video signal is said color signal and said flat panel display is said monochrome display, and otherwise storing said digital signals; and

timing control means in electrical communication with said universal video input selector means, said color reduction means, and said [stroage] storage means for controlling [the] processing of said video signal at [the] an [incomeing] incoming video rate, and controlling a reading of said [stroage] storage means for asynchronously outputting a stored one of said monochrome display image and said digital signals to said flat panel display at an outgoing video rate.

2. (Once Amended) An electronic control system receiving a video signal from a video signal source for visual presentation on a flat panel display, which comprises:

video input connector means for receiving composite and component video signals, and for generating a first code indicating a video [types] type of said video [signals] signal;

composite video converter means in electrical communication with said video input connector means for separating [color] chrominance [components] signals and luminance [components] signals from said video [signals] signal when said video type is composite ;

video input selector means in electrical communication with said video input connector means and said composite video converter means for selecting [between] said [color] chrominance [components] signals and said luminance [components] signals if said video [signals] type is composite, and for selecting said component video signals if said video type is component;

synchronization signal separation means in electrical communication with said video input [connection] connector means, said composite video converter means and said video input selector means

for extracting horizontal synchronization signals and vertical synchronization signals from said video [signals] signal as required by said video type;

A/D converter means in electrical communication with said video input selector means for receiving said [color] chrominance signals [components] and said luminance signals [components] from said video input selector means to produce digital [color] signals;

[Color] color to monochrome reduction means in electrical communication with said A/D converter means and receiving said digital [color] signals for mixing said digital [color] signals in accordance with weighting formulas to provide [monochrome-to-monochrome, monochrome-to-color,] color-to-monochrome[, and color-to-color] transition signals when said video signal is a color signal and said flat panel display is a monochrome display, and otherwise passing said digital signals through without reduction;

frame buffer means in electrical communication with said color-to-monochrome reduction means and said A/D converter means for storing received ones of said digital [color] signals and said color-to-monochrome transition signals at a first data rate and asynchronously outputting said received ones [said digital signals and said transition signals] at a second data rate compatible with said flat panel display;

microprocessor means in electrical communication with said video input connector means, said composite video converter means, said video input selector means, said synchronization signal separation means, said A/D converter means, and said color-to-monochrome reduction means, and receiving said first code and a second code, for determining video format[s] of said video signal[s] and a flat panel display type[s], and for controlling [the] operation of said electronic control means, and for supplying said weighting formulas to said color-to-monochrome reduction means;

pixel clock generator means in electrical communication with said microprocessor means, said synchronization signal separation means, and said A/D converter means, and responsive to said horizontal synchronization signals, said vertical synchronization signals, and said microprocessor means for generating pixel clock signals which are synchronized to said horizontal synchronization signals and supplied to said A/D converter means to control [the] processing of said video [signals] signal;

frame buffer input control means in electrical communication with said synchronization signal separation means, said frame buffer means, said pixel clock generator means, and said microprocessor

a1

means for controlling [the] storage of said digital [color] signals and said color-to-monochrome transition signals into said frame buffer means;

flat panel timing generator means in electrical communication with said microprocessor means, said [microprocessor means] frame buffer input control means, said pixel clock generator means, and said synchronization signal separation means for generating output control timing signals to drive said flat panel display, fit an image on said flat panel display, and control power sequencing in turning said electronic control system on and off as said video signal[s are] is received and interrupted;

image size/position control means in electrical communication with said microprocessor means, said frame buffer means, and said flat panel timing generator means for generating image control signals to control size, position and orientation of a video image presented on said flat panel display;

frame buffer output control means in electrical communication with said microprocessor means, said frame buffer means, and said image size/position control means for controlling addressing and output data rate of said received ones [said digital color signals and said transition signals] stored in said frame buffer means;

power circuit means in electrical communication with said microprocessor means for supplying power-up voltages to said electronic control system; and

flat panel interface module means in electrical communication with said microprocessor means, said flat panel timing generator means, said power circuit means, and said frame buffer means, and receiving said received ones [digital color signals and said transition signals] from said frame buffer means at said second data rate, said output control timing signals from said flat panel timing generator means, and a power-up voltage from said power circuit means, for routing said [digital color signals, said transition signals] received ones, said output control timing signals, and said power-up voltage to said flat panel display system, and for supplying said second code to said microprocessor means to identify [a] said flat panel display type.

4. The electronic control system of Claim 3, wherein said synchronization signal separation means includes a synchronization signal detector for locking onto said horizontal synchronization signals and said vertical synchronization signals.



69

4. (Once Amended) The electronic control system of Claim 3, wherein said video input connector means is a plug-in module which may be interchanged with selected ones of plural other plug-in modules to accommodate any type and format of said video [signals] signal.

5. (Once Amended) The electronic control system of Claim 3, wherein said [primary color components are] digital signals are comprised of red, green and blue color signals.

6. The electronic control system of Claim 3, wherein said video input connector means includes a selectably variable voltage reference to accommodate a wide range of amplitudes of said video signals.

7. (Once Amended) The electronic[s] control system of Claim 3, wherein said frame buffer means is comprised of plug-in frame buffer modules of varying bit length and frame size to accommodate a wide variety of video formats.

8. The electronic control system of Claim 3, wherein said electronic control system includes user controls in electrical communication with said microprocessor means for changing said weighting formulas and varying image contrast, position, brightness, and orientation, and shrinking and expanding said image on said flat panel display.

9. The electronic control system of Claim 8, wherein said user controls are comprised of analog controls, digital controls and configuration switches.

10. (Once Amended) The electronic control system of Claim 3, wherein said first data rate is an incoming video data rate and said second data rate is an asynchronous outgoing [at a] flat panel display data rate.

11. The electronic control system of Claim 3, wherein said A/D converter means is comprised of a pair of A/D converters per video color signal, wherein one of said pair of A/D converters digitizes even pixels and another of said pair of A/D converters digitizes odd pixels for accommodating high data rates.

12. The electronic control system of Claim 3, wherein said video types include VGA with said vertical synchronization signals and said horizontal synchronization signals separated, RS-170/RS-343 sync-on green, RS-170/RS-343 RGB separate composite sync, composite NTSC and PAL types, and said video formats include NTSC, PAL, HDTV, SECAM, XGA, SVGA, RGB, VGA 640 X 480 Graphics, VGA 80 X 25 Text, and VGA 640 X 350 Graphics.

14 ~~13.~~ The electronic control system of Claim 3 ~~2~~, wherein said microprocessor means determines said video formats on basis of number of said horizontal synchronization signals that are detected by said synchronization signal separation means for each of said vertical synchronization signals detected by said synchronization signal separation means, and polarity of said vertical synchronization signals and said horizontal synchronization signals.

15 ~~14.~~ The electronic control system of Claim 3 ~~2~~, wherein said electronic control system accommodates video resolutions up to at least 2048 X 2048 rows and columns.

16 ~~15.~~ The electronic control system of Claim 3 ~~2~~, wherein said video input connector means may be any one of a 15 pin VGA, BNC, or RCA type connectors.

17 ~~16.~~(Once Amended) The electronic control system of Claim 3 ~~2~~, wherein said flat panel interface module means is a plug-in [mode] module which may be interchanged with any selected one of plural other plug-in modules to accommodate any type of said flat panel display.

18 ~~17.~~(Once Amended)The electronic control system of Claim [2] 17 ~~16~~, wherein said plug-in module [may be] electrically communicates with any one of a color or monochrome LCD, electroluminescent, gas plasma or FED flat panel display.

19 18.(Once Amended)The electronic control system of Claim 3 ~~2~~ wherein said second code [may identify] identifies any one of at least 256 different flat panel display types.

20 ~~19.~~(Once Amended)The electronic control system of Claim 3 ~~2~~, wherein said video signal[s] may be any one of interlaced and non-interlaced video signals.

21 ~~20.~~ (Once Amended)A system for controlling [the] size, position and orientation of a video image presented on a flat panel display, and in electrical communication with a memory system having stored therein [a] said video image [for display on said flat panel display], and receiving a video signal from a video source, which comprises:

timing control means receiving said video signal from said video source at [said] a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first

clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining [said] a video signal resolution, and generating first control signals for reading said video image [information] in said memory system;

image size/position control means in electrical communication with said timing control means and responsive to said column start, row start, column replicate, and row replicate control signals and said first control signals for generating output column address control signals, [and] output row address control signals for said memory system[;] , and a pixel clock signal; and

frame buffer output control means in electrical communication with said timing control means, said memory system, said image size/position control means, and said flat panel display, and responsive to said pixel clock signal for reading said video image from said memory system.

~~21~~.(Once Amended)An analog-to-digital converter system for digitizing a video signal received from a video source at a high data rate, which comprises:

timing control means in electrical communication with said video source and receiving said video signal for generating a pixel clock signal in synchronization with a horizontal synchronization signal of said video signal;

a first analog-to-digital converter in electrical communication with said timing control means and said video source, and receiving said video signal and said pixel clock signal, and generating therefrom odd pixel data signals;

an inverter in electrical communication with said timing control means, and receiving said pixel clock signal, and producing an inverted pixel clock signal;

a second analog-to-digital converter in electrical communication with said inverter and said video source, and receiving said inverted pixel clock signal and said video signal, and generating therefrom [an] even pixel data signals; and

a two-to-one multiplexer in electrical communication with said first analog-to-digital converter, said timing control means, said inverter, and said second analog-to-digital converter, and interlacing said

odd pixel data signals and said even pixel data signals to produce a pixel signal representative of said video signal with no loss of resolution.

~~22.~~ (Once Amended)A system for reducing video color signals received from a video source to monochrome grey scale signals, which comprises:

digitizing means in electrical communication with said video source for digitizing said video color signals to produce a red digital color signal, a green digital color signal, and a blue digital color signal;

[an] AND gate logic means in electrical communication with said digitizing means and receiving said red digital color signal, said green digital color signal, and said blue digital color signal, for producing first logic signals;

memory means in electrical communication with said AND gate logic means and having stored therein weighting values for mixing said red digital color signal, said green digital color signal and said blue digital color signal;

microprocessor means in electrical communication with said memory means for storing said weighting values; and

OR gate logic means in electrical communication with said AND gate logic means and receiving said first logic signals to produce a monochrome grey scale video signal for presentation on said flat panel display.

~~23.~~ (Once Amended)A method of power-up and power down sequencing in an electronic control system for a flat panel display, said electronic control system having a first timing control system for generating digital synchronization signals, a second timing control system in electrical communication with said first timing control system for generating digital color signals and digital transition signals from a video signal received from a video source, a memory system in electrical communication with said first timing control system, said second timing control system, and said flat panel display, and having stored therein said digital color signals and said digital transition signals, and a backlight inverter power supply means in electrical communication with said first timing control system and said second timing control system, comprising the steps of :

supplying power to said flat panel display;

T1 seconds after supplying power to said flat panel display, [supplying power to] applying synchronizations signals from said first timing control system to said flat panel display;

T2 seconds after supplying power to said flat panel display, applying said digital color signals and said digital transition signals [supplying power to said second timing control system and] from said memory system to said flat panel display;

T3 seconds after supplying power to said flat panel display, supplying power to said backlight inverter power supply means;

When power to said electronic control system is to be turned off, turning off [the] power to said backlight inverter power supply means first;

T4 seconds after power to said backlight inverter power supply means is turned off, turning power to said [second timing control system and said] memory system off;

T5 seconds after power to said backlight inverter power supply means is turned off, turning power to said first timing control system off; and

T6 seconds after power to said backlight inverter power supply means is turned off, turning power to said flat panel display off.

Please add the following Claims:

--~~24~~. The electronic control system of Claim 1, wherein said universal video input selector means is comprised of any one of plural plug-in connectors including 15 pin VGA, BNC, and RCA type connectors, each of which has a unique code identifying said any one video type of said video signal.

--25, The method of Claim ~~23~~ 24, wherein the step of supplying power to said flat panel display occurs when said video signal is received, and the step of turning off power to said backlight inverter power supply means occurs when said video signal is no longer received.

--26. An electronic control system receiving a video signal from a video signal source and forming therefrom a display image for visual presentation on a flat panel display, which comprises:

a first timing control system for identifying a video type and a video format, for separating chrominance signals, luminance signals, and synchronization signals from said video signal, for separating primary color signals from said chrominance signals, for separating vertical synchronization signals and horizontal synchronization signals from said synchronization signals, and for reducing said primary color signals into digital transition signals as required by said video type for storage at a video rate of said video signal to form a display image;

a second timing control system in electrical communication with said first timing control system and said flat panel display, and responsive to said vertical synchronization signals and said horizontal synchronization signals for determining image parameters and a flat panel video rate for said flat panel display, and for positioning, orienting, and sizing said display image; and

a memory system in electrical communication with said first timing control system and said second timing control system for receiving said digital transition signals at said video rate, and asynchronously outputting said display image to said flat panel display at said flat panel video rate.

--27. A method of receiving a video signal having any one of plural video types and any one of plural video formats, and displaying said video signal on a flat panel display, which includes the steps of:

identifying said one of plural video types and said one of plural video formats of said video signal;

separating luminance signals, chrominance signals, and synchronization signals from said one of plural video types, and red component signals, green component signals, and blue component signals from said chrominance signals, and vertical synchronization signals and horizontal synchronization signals from said synchronization signals;

reducing said red component signals, said green component signals, and said blue component signals in accordance with one of plural weighting formulas to produce a first monochrome video signal if said video signal is a color video signal and said flat panel display is a monochrome display, and otherwise passing said red component signals, said green component signals, and said blue component signals through without reduction;

in response to said vertical synchronization signals and said horizontal synchronication signals for said one of said plural video formats, and at a first video rate of said video signal, and as one of interlaced and non-interlaced signals, receiving said first monochrome video signal if said video signal is said color video signal and said flat panel display is said monochrome display, receiving said color video signal if said flat panel display is a color display, and receiving said video signal if said video signal is a second monochrome video signal and said flat panel display is said monochrome display or said color display, thereby forming a display image; and

positioning, sizing, and orienting said display image while transferring said display image to said flat panel display asynchronously at a flat panel video rate.

--28. The method of Claim 27, wherein said display image is one or more of an upside down image form, a portrait image form, a mirror-image form, and a rotated image form.



75

--29. The method of Claim 27, wherein said plural weighting formulas are comprised of the following:

| | | | |
|---|---|---|---|
| NTSC WEIGHTING | 5/16 Red | 9/16 Green | 2/16 Blue |
| EQUAL WEIGHTING | 5/16 Red | 6/16 Green | 5/16 Blue |
| GREEN ONLY | 0/16 Red | 16/16 Green | 0/16 Blue |

--30. The method of Claim 27, wherein said plural video types are comprised of composite video and component video types, and said plural video formats are comprised of all RGB video formats including VGA, SVGA, XGA, NTSC, PAL, and SECAM.

--31. The method of Claim 27, wherein said flat panel display is one of LCD, electroluminescent, gas plasma, and FED display.

--32. The method of Claim 27, wherein said plural video types are up to 256 in number, and include VGA with separate HSYNC and VSYNC, RS-170/RS-343 RGB Sync-On-Green, RS-170/RS-343 RGB Separate Composite Sync, Composite Video (NTSC/PAL), and Computer Video (HDTV).

--33. The method of Claim 27, wherein said plural video formats include NTSC, PAL, HDTV, VGA 640 x 480 Graphics, VGA 80 x 25 Text, and VGA 640 x 350 Graphics.

--34. The method of Claim 27, wherein said first video rate is slower than and asynchronous to said flat panel video rate.

--35. The method of Claim 27, wherein said first video rate is faster than and asynchronous to said flat panel video rate.

--36. The method of Claim 27, wherein said step of reducing occurs in accordance with the following general equation:

Monochrome Data [bits 0-7] = {Red Data [bits 0-7]}• {Red Weighting [bits 0-7]}
+ {Green Data [bits 0-7]}• {Green Weighting [bits 0-7]}
+ {Blue Data [bits 0-7]} • {Blue Weighting [bits 0-7]},

where "+" refers to a logical OR function and "•" refers to a logical AND function.--

IN THE SPECIFICATION

1. Please amend the title to the specification to read as follows: "Automated Flat Panel Display Control System For Accommodating Broad Range Of Video Types And Formats".

2. On page 3, line 41, before "timing" delete the article "a".

3. On page 11, line 8, change "Further" to "In addition".

4. In Table VIII on page 15, under the column captioned "PARAMETERS", in rows 1, 2 and 4, change "image start rows" to "image start row", and in row 4 also change "image start columns" to "image start column".